REMARKS

Claims 57-77, 79-87, and 90 are pending in the present application. Claims 57-90 were presented for examination. Claims 78, 88, and 89 have been cancelled by amendment.

In the office action mailed December 17, 2004 (the "Office Action"), claims 73 and 78, and the specification were objected to for informalities. Claims 58-60, 76, 78, 80, 81, 88, and 89 were also rejected in the Office Action under 35 U.S.C. 112, second paragraph. Claim 78 was further rejected under 35 U.S.C. 101. Claims 57-72, 77, 79, 82, and 83 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,712,883 to Miller *et al.* (the "Miller patent"). Claims 73-75 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 84-87 and 90 were allowed.

With respect to an Information Disclosure Statement ("IDS") submitted on April 25, 2001, applicant requests the Examiner consider all the references listed on the Form PTO-1449. Pursuant to MPEP 609 III.A(2), copies of all the cited references listed in this IDS do not need to be submitted since all of the references were provided in a prior application, U.S. Application No. 08/879,847, filed on June 20, 1997. The prior application was properly identified in the IDS and was relied on for an earlier filing date under 37 U.S.C. 120.

An IDS was also submitted on November 15, 2004. Applicant requests the Examiner consider the references cited in the Form PTO-1449 of the IDS and provide the attorney of record with a signed and initialed copy of the Form PTO-1449.

With respect to the objection to claim 73, claim 73 has been amended as suggested by the Examiner. Claim 78 has been cancelled, and consequently, the Examiner's objection to claim 78 is now moot. Additionally, the specification has been amended to complete the cross-reference information by providing the U.S. Patent Number and issue date, as suggested by the Examiner. In light of the amendments to claim 73 and the specification, the Examiner's objections have been overcome.

With respect to the Examiner's rejection of claim 58 under 35 U.S.C. 112, second paragraph, Applicant would like to clarify that Figure 3 illustrates only one embodiment of a command latch 200 and clock generator 210 according to the present invention. As well known, although the claims are read in light of the specification, the scope of the claims are not limited

to only the embodiments described in the specification. Thus, claim 57 is not limited to the specific embodiment shown in Figure 3. Claim 58 has been amended to clarify that "delay locking the reference clock signal to the master clock signal" recited in claim 57 comprises "delay locking the reference clock signal to the master clock signal so that the reference clock signal is locked to the same phase as the master clock signal." The support for claim 58 can be found at page 13, line 22-page 15, line 5, and Figures 3 and 4 of the present application. As described, in one embodiment of the invention, the signal E0 has substantially the same phase as the clock signal at the output of the receiver buffer. Assuming that the E0 signal represents the reference clock signal, and the clock signal output by the receiver buffer represents the master clock signal, claim 58, which recites that the reference clock signal is locked to the same phase as the master clock signal, then claim 58 is supported by the specification and drawings.

Claim 59 has also been amended to clarify that the delay locking of the reference clock signal to the master clock signal comprises locking the two signals to have the same phase, and further that delay locking the plurality of clock signals to the reference clock signal comprises delay locking one of the clock signals to have an opposite phase of the reference signal, and that the remainder of the clock signals have respective phases that are spaced from each other between the phases of the reference clock signal and the one clock signal. Claim 59 is supported by the same material cited with respect to supporting claim 58.

With respect to claim 76, claim 76 has been amended to clarify that the limitations of generating a first signal, generating a second signal, and generating a control signal are directed to refining the limitation of delay locking the one of the clock signals to the master clock signal, recited in claim 66. Claims 80 and 81 have been similarly amended to clarify that the dependent claims are directed to the limitations of generating the first control signal and generating the second control signal, respectively, recited in claim 77. Claims 78, 88, and 89 have been cancelled, and thus, the rejection of claims 88 and 89 is now moot.

For the foregoing reasons, the rejection of claims 58, 59, 76, 80, and 81 under 35 U.S.C. 112, second paragraph, should be withdrawn.

With respect to the rejection of claim 78 under 35 U.S.C. 101, claim 78 has been cancelled, as previously mentioned, and consequently, the rejection is no longer relevant.

Claims 57-72, 77, 79, 82, and 83 have been rejected under 35 U.S.C. 102(e), as previously mentioned, as being anticipated by the Miller patent.

The Miller patent is directed to a clock signal distribution system 10 having a plurality of deskewing stages 16(1)-16(N) for generating N local clock signals CLKL(1)-CLKL(N). All of the local clock signals CLKL(1)-CLKL(N) have the same phase as a periodic reference signal CLKA(1). *See* col. 4, lines 7-16. In this manner, all of the local modules 12(1)-12(N), can operate synchronously with respect to the reference clock signal CLKA(1). As described in the Miller patent, an object of the clock signal distribution system 10 is "to provide a set of synchronized local clock signals [CLKL(1)-CLKL(N)] to spatially distributed circuit modules." *See* col. 3, lines 27-30.

Claims 57, 61, 66, and 77 are patentably distinct from the Miller patent because the Miller patent fails to disclose the combination of limitations recited by the respective claims. For example, claim 57 recites a method of generating a sequence of clock signals that includes delay locking a plurality of clock signals to the reference clock signal, the plurality of clock signals have different respective phases relative to the phase of the reference clock signal. As previously discussed, the Miller patent discloses a clock signal for generating a plurality of clock signals CLKL(1)-CLKL(N) that are all *in phase* with the reference clock signal CLKA(1). As described in the Miller patent, the intended use of the clock signal distribution system described therein is to provide local clock signals to a plurality of spatially distributed circuit modules, which is accomplished by providing the plurality of deskewing stages 16(1)-16(N) to generate the synchronized local clock signals CLKL(1)-CLKL(N) that have the same phase as a reference clock signal CLKA(1).

Similarly, claim 61 recites a method of generating a sequence of clock signals from a master clock signal including generating the sequence of clock signals, each signal of the sequence having a different respective phase that increases from a first clock signal to a last clock signal in the sequence. In contrast, the clock signal distribution system disclosed in the Miller patent generates a plurality of local clock signals CLKL(1)-CLKL(N) that are all in phase with a reference clock signal CLKA(1). That is, each of the local clock signals CLKL(1)-CLKL(N) have the same phase as the reference clock signal CLKA(1).

Claim 66 recites a method of generating a sequence of clock signals including delay locking one of the clock signals of the sequence to a master clock signal, the clock signals in the sequence have different respective phases with respect to the master clock signal. Claim 77 recites a method for providing a plurality of clock signals that have predetermined phases relative to a master clock signal that includes producing the plurality of clock signals having different respective phases relative to the reference clock signal. As previously discussed with respect to claims 57 and 61, the Miller patent fails to at least disclose the generation of clock signals, each having a different respective phase relative to either the reference clock signal or the master clock signal. The Miller patent is directed to a clock signal distribution system for providing a plurality of local clock signals CLKL(1)-CLKL(N) having the same phase as a reference clock signal CLKA(1). As stated in the Miller patent, the object of the invention is to provide local clock signals that are in phase with a reference clock signal to spatially distributed circuit modules in order for the circuit modules to operate synchronously with respect to the reference clock signal.

For the foregoing reasons, claims 57, 61, 66, and 77 are patentably distinct from the Miller patent. Claims 58-60, which depend from claim 57, claims 62-65, which depend from claim 61, claims 67-76, which depend from claim 66, and claims 79-83, which depend from claim 77, are similarly patentably distinct from the Miller patent based on their dependency from a respective allowable base claim. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. Therefore, the rejection of claims 57-72, 77, 79, 82, and 83 under 35 U.S.C. 102(e) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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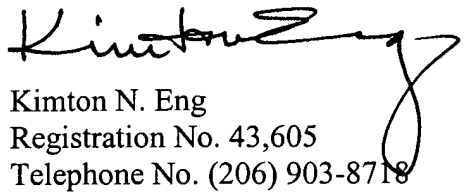

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